NXP Introduces High Performance, Arm Cortex-M33 / DSP Crossover Processor with 4.5MB on-chip SRAM

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i.MX RT600 hits optimal balance in power, performance, and memory for deeply embedded machine learning and next-generation localized voice assistants

San Jose, California – (ARMTECHCON2018) – October 10, 2018 – NXP Semiconductors is announcing i.MX RT600, a breakthrough family of crossover processors for ultra-low power secure Machine Learning (ML) / Artificial Intelligence (AI) edge applications, including performance-intensive far-field voice input and immersive 3D audio playback.

The i.MX RT600 is a multi-core crossover processor family, which features up to 300 MHz Arm® Cortex®-M33 and a 600 MHz Cadence® Tensilica® HiFi 4 audio/voice digital signal processor (DSP) with four MACS and hardware-based transcendental and activation functions. Leveraging 28nm FD-SOI technology, i.MX RT600 supports the high-performance cores with 4.5MB of on-chip low-leakage SRAM, which has been configured for simultaneous zero-wait state access – ideal for real-time execution of audio/voice, machine learning, and neural network-based applications.

The i.MX RT600 family integrates benchmark security features, such as secure boot with immutable hardware 'root-of-trust,' and SRAM Physically Unclonable Function (PUF) based unique key storage, certificate-based secure debug authentication, AES-256 & SHA2-256 acceleration, and DICE security standard implementation for secure cloud-to-edge communication. The public key infrastructure (PKI), or asymmetric cryptography, is further accelerated by the dedicated asymmetric accelerator for ECC and RSA algorithms. In addition to SRAM PUF, i.MX RT600 includes an optional fuse-based root key storage mechanism for secure boot and crypto operations.

One of the key features of the Arm Cortex-M33 is the dedicated co-processor interface that extends the processing capability of the CPU by allowing efficient integration of tightly-coupled co-processors while maintaining full ecosystem and toolchain compatibility. NXP has utilized this capability to implement a co-processor for accelerating key ML and DSP functions, such as, convolution, correlation, matrix operations, transfer functions, and filtering; enhancing performance by up to 10x compared to executing on Arm Cortex-M33. The co-processor further leverages the popular CMSIS-DSP library calls (API) to simplify customer code portability.

For improved power efficiency, the on-chip SRAM can be partitioned into 30 shared configurable blocks of memory to ensure routines and I/O do not contest bus time. Each partition can be independently placed in a low-power retention mode or powered off entirely to reduce leakage. The HiFi 4 also has 64K of tightly coupled instruction and data memory (TCM), and optimized instruction and data cache for executing out of the shared SRAM. There is additional off-chip memory extension through a quad/octal SPI flash interface, optimized with an on-the-fly decryption engine and 8KB cache.

This family of crossover processors includes an audio/voice subsystem with support of up to eight DMIC channels, with hardware for Voice Activation Detect (VAD), and up to eight I2S peripherals. Additional peripherals include SDIO for wireless communication, high speed USB with on-chip PHY, 12-bit ADC with temperature sensor, and numerous serial interfaces including 50 Mbps SPI, I3C, and six configurable serial interfaces (USART, SPI, I2C or I2S) with individual FIFO and DMA service request support.

Product Demonstration

NXP will be demonstrating the voice capabilities of the i.MX RT600 family at Arm TechCon with DSP Concepts and Sensory. Find us in booth #620.

For more information, please visit www.nxp.com/iMXRT600.